Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
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L2	0	matrix DAC cell digital sampling latching interval	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	WITH	ON	2005/06/07 08:05
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L5	0	matrix DAC cell digital sample interval	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	SAME	ON	2005/06/07 08:08
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L7	4	matrix DAC cell digital sample	USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	SAME	ON	2005/06/07 08:12
L8	0	matrix DAC cell sampling	USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	SAME	ON	2005/06/07 08:13
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L12	4	DAC matrix sampling interval	USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	SAME	ON	2005/06/07 08:15
L13	6	DAC matrix sample interval	USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	SAME	ON	2005/06/07 08:17
L14	2	DAC cell sampling interval	USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	SAME	ON	2005/06/07 08:17
L15	3	DAC cell sampling latch	USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	SAME	ON	2005/06/07 08:51
L16	1	"6650266"	USPAT	OR	OFF	2005/06/07 08:51
L17	363181	"6650266" gate	USPAT	OR	ON	2005/06/07 08:51
L18	0	"6650266" gate	USPAT	AND	ON	2005/06/07 08:51
L19	0	"6650266" "and"	USPAT	AND	ON	2005/06/07 08:51
L20	1	"6650266" "70"	USPAT	AND	ON	2005/06/07 09:13
L21	4531	((341/143,136,144,153,162) or (257/197,327,139,140,141,138, 136,256)).CCLS.	USPAT	OR	OFF	2005/06/07 09:14

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1 Automated layout generation using gate matrix approach

Y.-C. Chang, S.-C. Chang, L.-H. Hsu

October 1987 **Proceedings of the 24th ACM/IEEE conference on Design automation**

Full text available: pdf(683.06 KB) Additional Information: full citation, abstract, references, citings, index terms

This paper presents a software system ALSUGMA for automated gate matrix layout generation. Its structured Net-List and Realization Matrix models which are different from previous interval graph approach are introduced. Algorithms to minimize and realize the gate matrix layout are also presented with examples. Empirical results showed good performance in terms of both speed and layout quality. Folding technique for such layout style is also introduced.

2 Cell generators: PARAGON: a new package for gate matrix layout synthesis

R. Burgess, C. Wouters

March 1990 **Proceedings of the conference on European design automation**

Full text available: pdf(522.98 KB) Additional Information: full citation, abstract, references

Gate matrix is a layout style for implementing logic in integrated MOS circuits. In this paper we discuss algorithms used in a newly developed software package called PARAGON which generates near-optimal gate matrix geometric layouts given a set of logic expressions. New features include individual sizes of transistors being taken into account at all stages of the algorithms and the use of transistor orientations to reduce the width and improve the timing performance of the gate matrix layouts. ...

Keywords: cell generation, gate-matrix layout, logic synthesis, optimisation, physical design, placement, routing, simulated annealing

3 Array optimization for VLSI synthesis

D. F. Wong, C. L. Liu

October 1987 **Proceedings of the 24th ACM/IEEE conference on Design automation**

Full text available: pdf(583.15 KB) Additional Information: full citation, abstract, references, citings, index terms

We present in this paper an algorithm that solves a general array optimization problem. The algorithm can be used for compacting Gate Matrix layouts, SLA's, Weinberger Arrays, and for multiple folding of PLA's. Our approach is based on the technique of simulated

annealing. A major contribution of this paper is the formulation of the solution space which facilitates an effective search for an optimal solution. Experimental results are very encouraging.

4 ALPS2: a standard cell layout system for double-layer metal technology
C. P. Hsu, B. N. Tien, K. Chow, R. A. Perry, J. Tang
June 1985 **Proceedings of the 22nd ACM/IEEE conference on Design automation**

Full text available: pdf(605.60 KB) Additional Information: full citation, abstract, references, citings, index terms

A layout style for double-layer metal standard cell design is described. Based on this particular style, an automatic layout system (ALPS2) is developed. It mixes state of the art placement and routing techniques in different stages of the layout process, which deviates from the traditional place-first-then-route strategy, and produces efficient results. The chip area comparisons between three single layer metal standard cell designs and those of the ALPS2 system showed up to 18% reduction ...

5 MGX: An integrated symbolic layout system for VLSI
Masaru Ozaki, Miho Watanabe, Morio Kakinuma, Mikio Ikeda, Koji Sato
June 1984 **Proceedings of the 21st conference on Design automation**

Full text available: pdf(658.73 KB) Additional Information: full citation, abstract, references, citings, index terms

A symbolic layout system for double-metal silicon-gate MOS technology in the style of Gate Matrix is presented. This system provides an integrated layout environment which consists of stick-figure-based graphic editor, a mask artwork generator, a connectivity checker, a circuit parameter extracter and simulator interfaces. All the modules are designed to deal with symbol data, rather than mask artwork, so that fast execution is realized. A method to associate symbol data with actual mask ge ...

6 Module compaction in FPGA-based regular datapaths
Andreas Koch
June 1996 **Proceedings of the 33rd annual conference on Design automation**

Full text available: pdf(367.14 KB) Additional Information: full citation, references, citings, index terms

7 Chip assembly in the PLAYOUT VLSI design system
Klaus Glasmacher, Gerhard Zimmermann
November 1992 **Proceedings of the conference on European design automation**

Full text available: pdf(839.75 KB) Additional Information: full citation, references, citings, index terms

8 Gate matrix layout synthesis with two-dimensional folding
I. Lin, D. H. C. Du, S. H. C. Yen
June 1989 **Proceedings of the 26th ACM/IEEE conference on Design automation**

Full text available: pdf(850.00 KB) Additional Information: full citation, abstract, references, index terms

We have developed a gate matrix layout synthesis tool which utilizes folding technique on both rows and columns. The conventional interval graph model and the recently proposed dynamic net-list representation can not fully depict circuit schematics such as inter-net connections. The incomplete representations may mislead the search process for an optimal solution during the layout partitioning and the gate ordering phases. We propose a new graph-based model called hierarchical dynamic net-l ...

9 PALACE: a layout generator for SCVS logic blocks
Knut M. Just, Edgar Auer, Werner L. Schiele, Alexander Schwaferts
January 1991 **Proceedings of the 27th ACM/IEEE conference on Design automation**

Full text available: pdf(856.11 KB) Additional Information: full citation, abstract, references, index terms

A novel approach to the automatic layout synthesis of dynamic CMOS circuits is presented. A set of logic expressions is realized in a row of cells. Taking multi-level Boolean expressions as input, logic transistors are placed and routed. Efficient solutions are achieved by permuting the variables of the expressions and by row folding. The layout is designed on a coarse grid taking timing requirements into account and afterwards adapted to the geometric design rules by a compactor. A compari ...

10 Dedicated circuits: A programmable cellular neural network circuit
Michel Leong, Pedro Vasconcelos, Jorge R. Fernandes, Leonel Sousa
September 2004 **Proceedings of the 17th symposium on Integrated circuits and system design**

Full text available: pdf(695.99 KB) Additional Information: full citation, abstract, references, index terms

In this paper we propose and develop a fully programmable CNN circuit. The CNN coefficients are digitally programmable using a Digital to Analog Converter (DAC), resulting in added flexibility.CNNs with 4x4 and 16x16 cells are designed and tested, exhibiting good accuracy when compared with Matlab and Java applications for computing CNNs.All circuits are designed and implemented with a 0.35um CMOS technology. The layout of a full 4x4 CNN was designed using Cadence Design Framework II. The circui ...

Keywords: VLSI, cellular neural networks, microelectronics

11 Hierarchical Simulation of Substrate Coupling in Mixed-Signal ICs Considering the Power Supply Network
T. Brandtner, R. Weigel
March 2002 **Proceedings of the conference on Design, automation and test in Europe**

Full text available: pdf(132.25 KB) Publisher Site Additional Information: full citation, abstract

This paper presents a novel substrate coupling simulationtool that is well suited to floorplanning of large mixed-signalIC designs. The IC layout may consist of severalsubcircuits, hence a hierarchical design flow, which is usuallyused for IC circuit design and layout, is supported.Coupling data modelling the substrate inside subcircuitsare precalculated and subsequently used during floorplanningleading to shorter simulation time. In addition, theimpedance model of the power grid is considered a ...

12 A fast and accurate characterization method for full-CMOS circuits
R. Peset Llopis, H. G. Kerkhoff
November 1992 **Proceedings of the conference on European design automation**

Full text available: pdf(684.01 KB) Additional Information: full citation, references, index terms

13 Automatic floorplan design
Ralph H.J.M. Otten
January 1982 **Proceedings of the 19th conference on Design automation**

Full text available: pdf(723.16 KB) Additional Information: full citation, abstract, references, citings, index terms

The problem of allocating area to modules at the highest level of a top-down decomposition

is treated in this paper. A theorem of Schoenberg is applied to obtain a good embedding of the module space into the plane. The dutch metric is introduced to transform netlist information - if available - into a distance matrix. This metric is flexible enough to enable the user to steer the design in an interactive environment, and rigorous enough to yield results satisfying optimality criterions. The ...

14 Placement: Temperature-aware global placement

Bernd Obermeier, Frank M. Johannes
January 2004

Full text available: pdf(477.04 KB) Publisher Site

Additional Information: full citation, abstract, references

This paper describes a deterministic placement method for standard cells which minimizes total power consumption and leads to a smooth temperature distribution over the die. It is based on the Quadratic Placement formulation, where the overall weighted net length is minimized. Two innovations are introduced to achieve the above goals. First, overall power consumption is minimized by shortening nets with a high power dissipation. Second, cells are spread over the placement area such that the die ...

15 A "gridless" variable-width channel router for marco cell design

C. H. Ng
October 1987 **Proceedings of the 24th ACM/IEEE conference on Design automation**

Full text available: pdf(458.50 KB)

Additional Information: full citation, abstract, references, citings, index terms

In this paper, we present a channel router especially designed for routing macro cells. The router routes variable-width pins with wires of any width. Although the router uses a routing grid internally, it acts like it is completely gridless to the user. Pins along the top and the bottom edges of the channel can be at any X-location, and the router uses a channel compactor to compact all horizontal segments vertically. The router allows pins to be on either of the two routing layers. If all ...

16 Schedulability analysis of multiprocessor real-time applications with stochastic task execution times

Sorin Manolache, Petru Eles, Zebo Peng
November 2002 **Proceedings of the 2002 IEEE/ACM international conference on Computer-aided design**

Full text available: pdf(107.76 KB)

Additional Information: full citation, abstract, references, citings, index terms

This paper presents an approach to the analysis of task sets implemented on multiprocessor systems, when the task execution times are specified as generalized probability distributions. Because of the extreme complexity of the problem, an exact solution is practically impossible to be obtained even for toy examples. Therefore, our methodology is based on approximating the generalized probability distributions of execution times by Coxian distributions of exponentials. Thus, we transform the gene ...

17 The $UCON_{ABC}$ usage control model

Jaehong Park, Ravi Sandhu
February 2004 **ACM Transactions on Information and System Security (TISSEC)**, Volume 7 Issue 1

Full text available: pdf(518.61 KB)

Additional Information: full citation, abstract, references, citings, index terms

In this paper, we introduce the family of $UCON_{ABC}$ models for usage control (UCON), which integrate *Authorizations (A), oBligations (B), and Conditions (C)*. We call these core models

because they address the essence of UCON, leaving administration, delegation, and other important but second-order issues for later work. The term usage control is a generalization of access control to cover authorizations, obligations, conditions, continuity (ongoing controls), and mutability. Trad ...

Keywords: access control, digital rights management, privacy, trust, usage control

18 Wire packing: a strong formulation of crosstalk-aware chip-level track/layer assignment with an efficient integer programming solution

Rony Kay, Rob A. Rutenbar

May 2000 **Proceedings of the 2000 international symposium on Physical design**

Full text available: pdf(292.95 KB) Additional Information: full citation, references, citings

19 Static timing analysis including power supply noise effect on propagation delay in VLSI circuits

Geng Bai, Sudhakar Bobba, Ibrahim N. Hajj

June 2001 **Proceedings of the 38th conference on Design automation**

Full text available: pdf(242.00 KB) Additional Information: full citation, abstract, references, citings, index terms

This paper presents techniques to include the effect of supply voltage noise on the circuit propagation delay of a digital VLSI circuit. The proposed methods rely on an input-independent approach to calculate the logic gate's worst-case power supply noise. A quasi-static timing analysis is then applied to derive a tight upper-bound on the delay for a selected path with power supply noise effects. This upper-bound can be further reduced by considering the logic constraints and dependencies ...

20 MILD - A cell-based layout system for MOS-LSI

Koji Sato, Takao Nagai, Mikio Tachibana, Hiroyoshi Shimoyama, Masaru Ozaki, Toshihiko Yahara

June 1981 **Proceedings of the 18th conference on Design automation**

Full text available: pdf(773.66 KB) Additional Information: full citation, abstract, references, citings, index terms

A standard-cell-based layout system for MOS-LSI termed MILD is reported. MILD has several features which seem to be profitable from the practical viewpoint of LSI developers; one of them is that macro blocks such as memory cells can be contained in the chip laid out.

Results 1 - 20 of 90 Result page: **1** 2 3 4 5 next